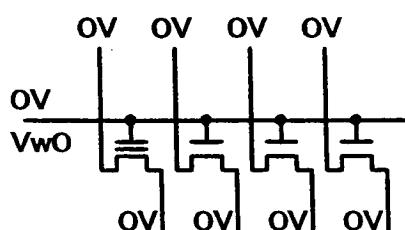


FIG. 1A

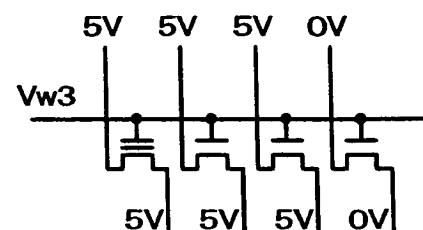
INITIAL STATE



	00	01	10	11
WRITE TARGET DATA	00	01	10	11
MEMORY CELL DATA	00	00	00	00
DISTURBANCE	-	-	-	-

FIG. 1B

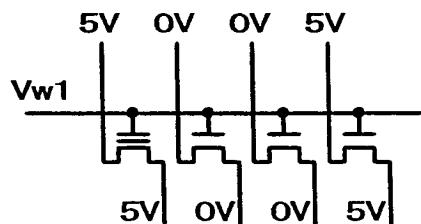
WRITE #1



	00	01	10	11
WRITE TARGET DATA	00	01	10	11
MEMORY CELL DATA	00	00	00	11
DISTURBANCE	++	-	-	-

FIG. 1C

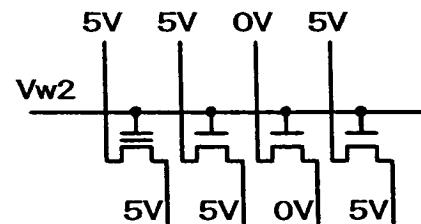
WRITE #2



	00	01	10	11
WRITE TARGET DATA	00	01	10	11
MEMORY CELL DATA	00	01	01	11
DISTURBANCE	++	-	-	+

FIG. 1D

WRITE #3



	00	01	10	11
WRITE TARGET DATA	00	01	10	11
MEMORY CELL DATA	00	01	10	11
DISTURBANCE	++	++	-	+

FIG. 1E

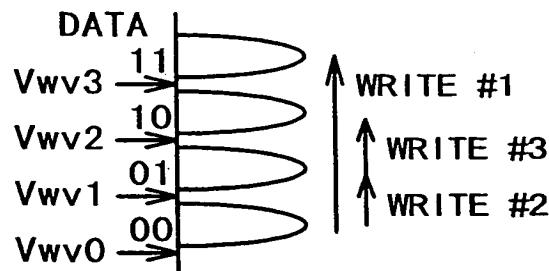


FIG. 2A

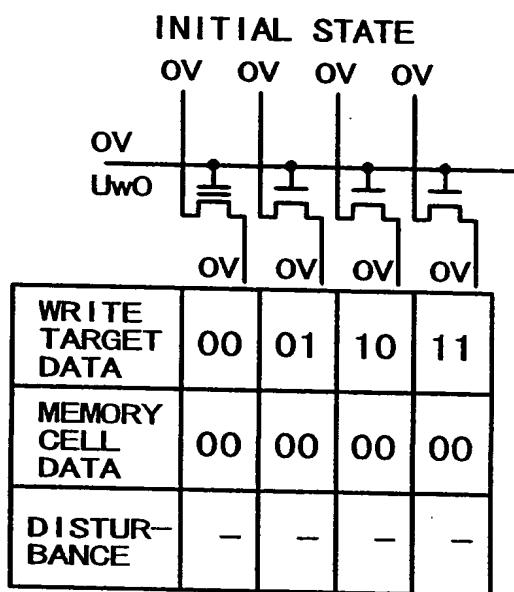


FIG. 2B

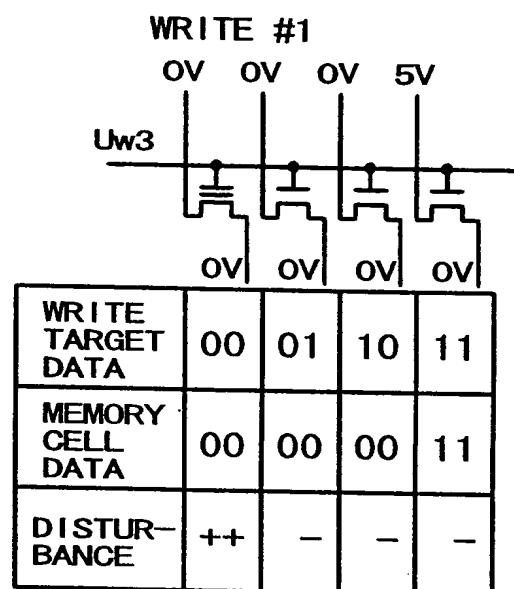


FIG. 2C

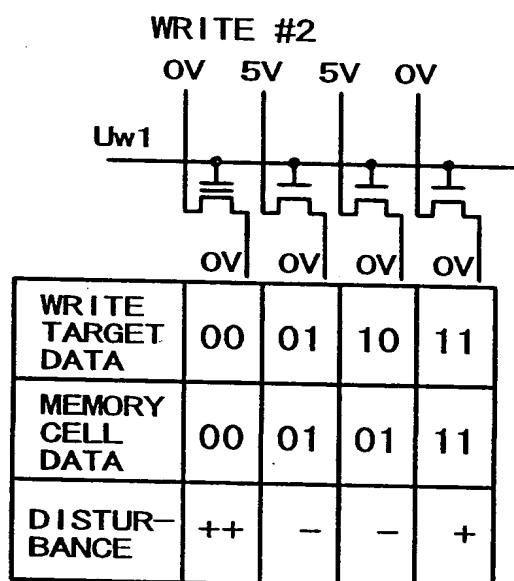


FIG. 2D

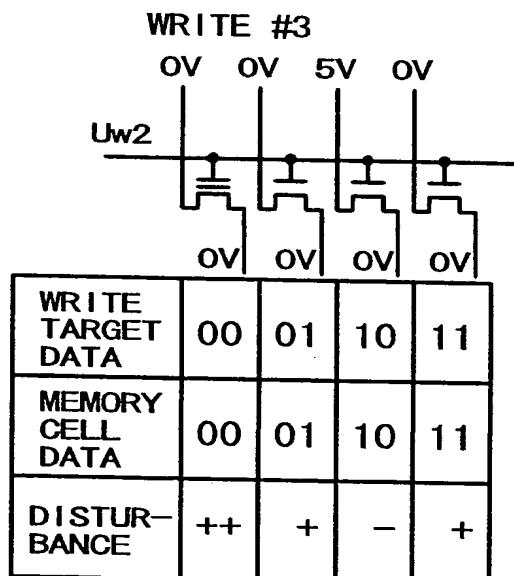


FIG. 2E

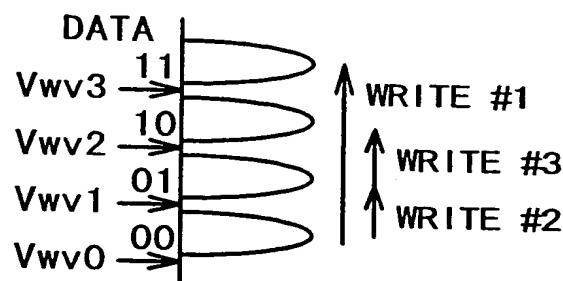


FIG. 3A (PRIOR ART)

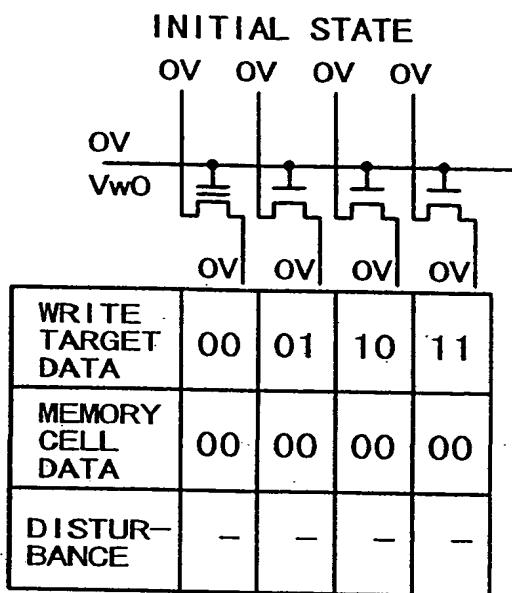


FIG. 3B (PRIOR ART)

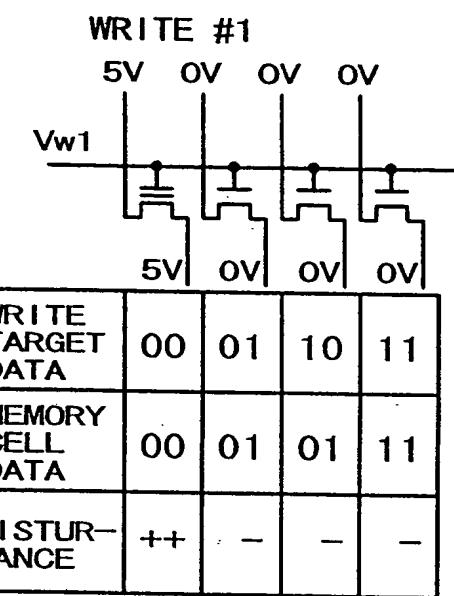


FIG. 3C (PRIOR ART)

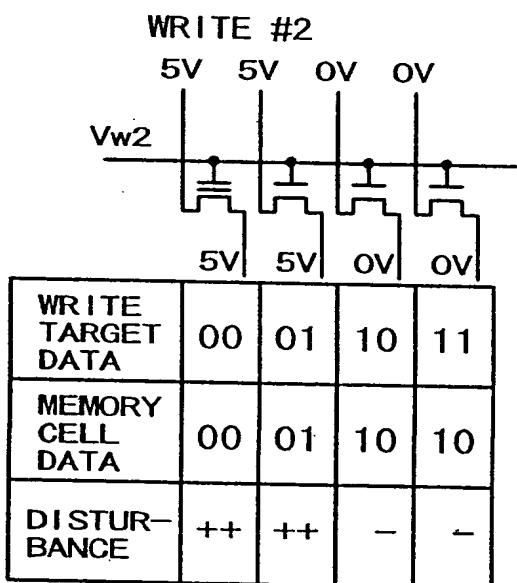


FIG. 3D (PRIOR ART)

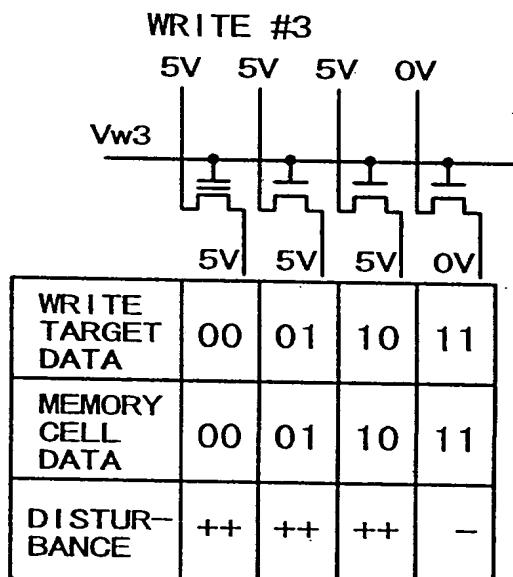


FIG. 3E (PRIOR ART)

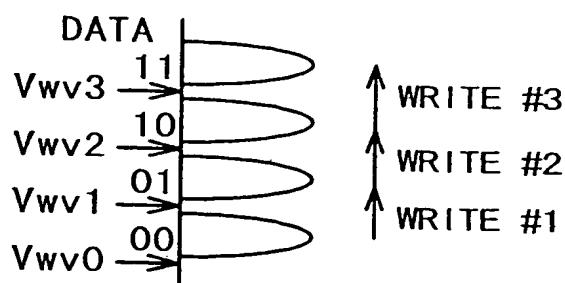


FIG. 4A (PRIOR ART)

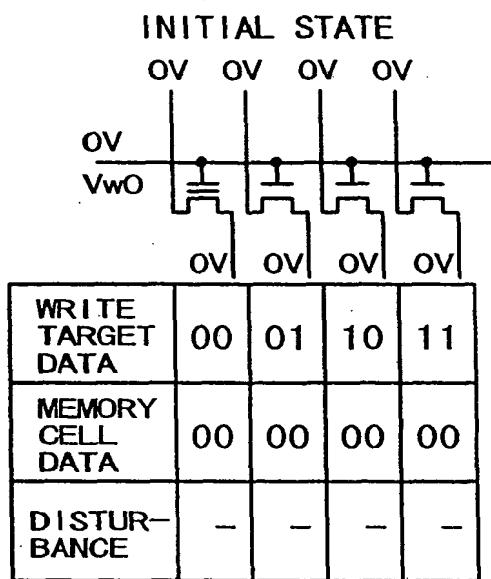


FIG. 4B (PRIOR ART)

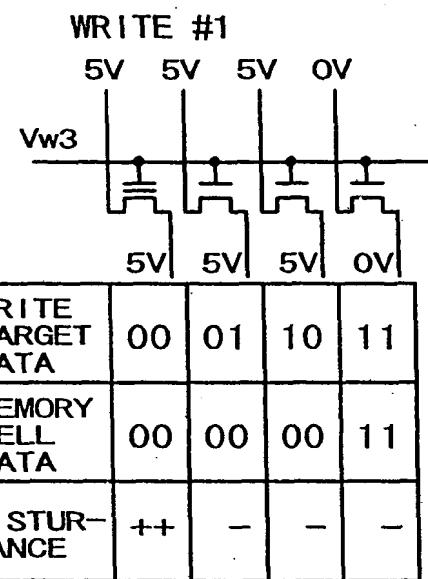


FIG. 4C (PRIOR ART)

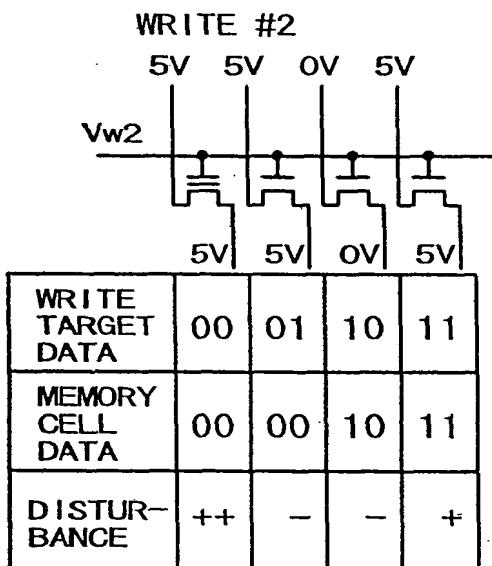


FIG. 4D (PRIOR ART)

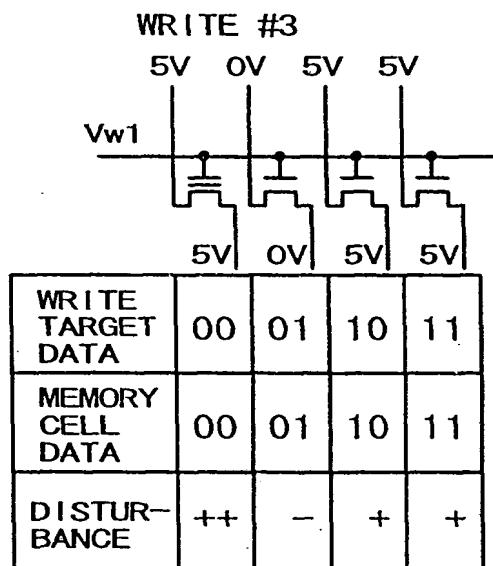


FIG. 4E (PRIOR ART)

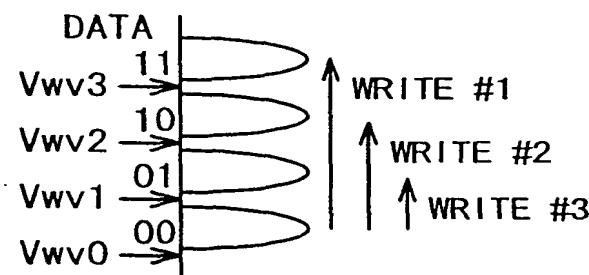


FIG. 5A (PRIOR ART)

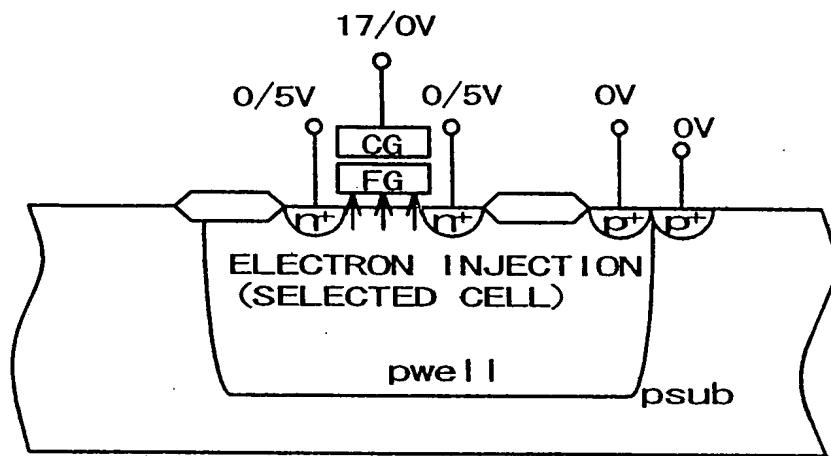


FIG. 5B (PRIOR ART)

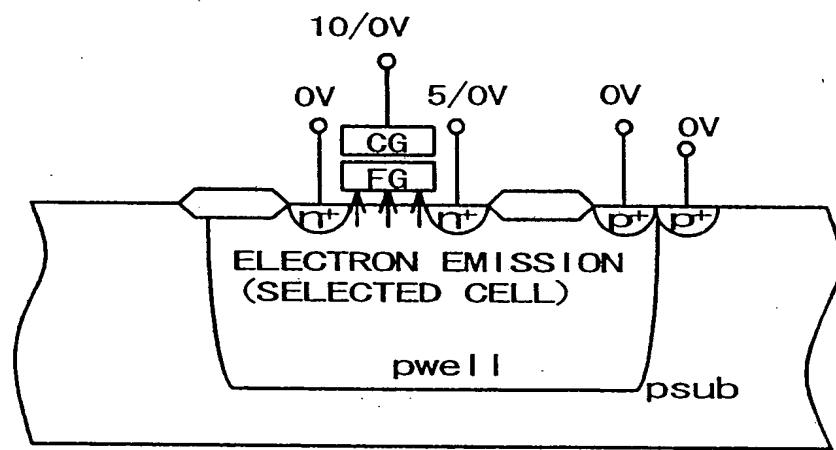


FIG. 6 (PRIOR ART)

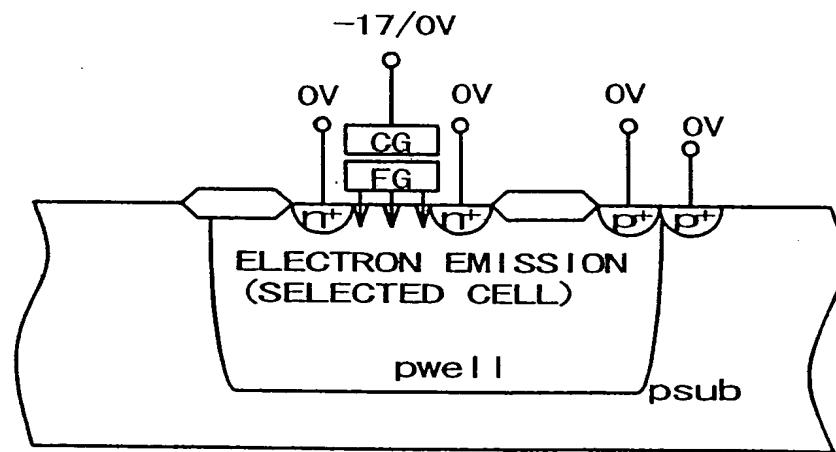


FIG. 7

	PRESENT INVENTION	PRIOR ART 1	PRIOR ART 2
WRITE #1	1	13	1
WRITE #2	13	21	27
WRITE #3	21	1	13
PULSES	35	35	41

FIG. 8

	PRESENT INVENTION	PRIOR ART 1	PRIOR ART 2
WRITE TIME PERIOD	1449 μ SECONDS	1449 μ SECONDS	1695 μ SECONDS
"00" LEVEL DISTURBANCE	0. 381V	0. 382V	0. 382V
"01" LEVEL DISTURBANCE	0. 001V	0. 097V	0. 000V
"10" LEVEL DISTURBANCE	0. 000V	0. 017V	0. 000V
"11" LEVEL DISTURBANCE	0. 000V	0. 000V	0. 000V

FIG. 9

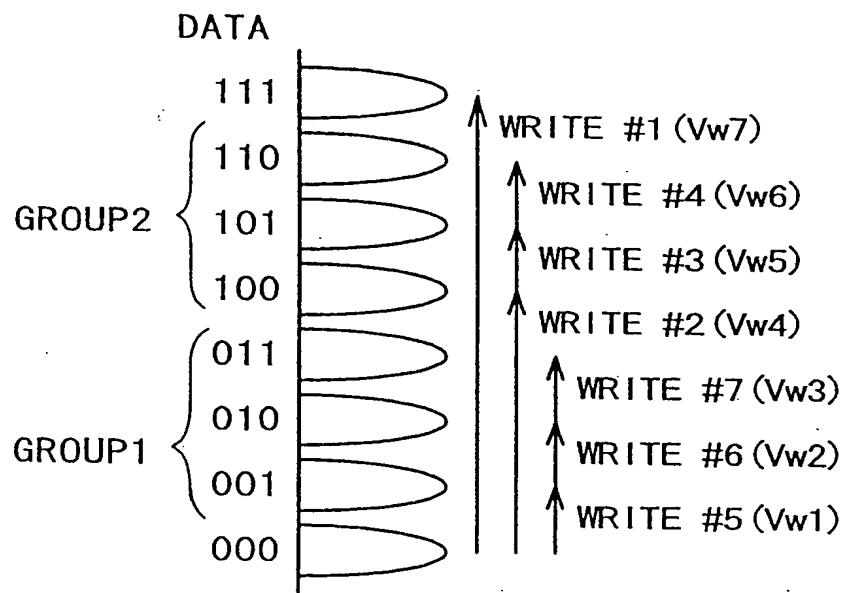


FIG. 10

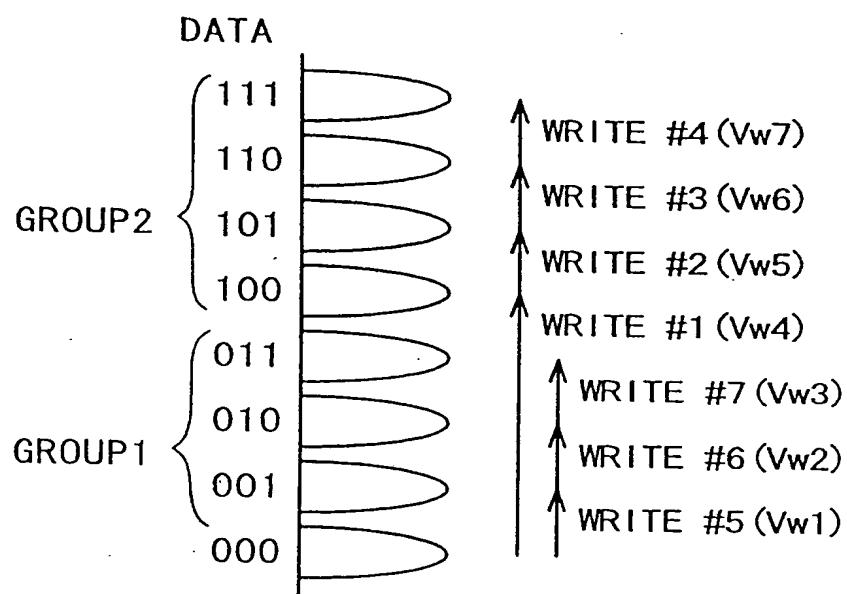


FIG. 11A

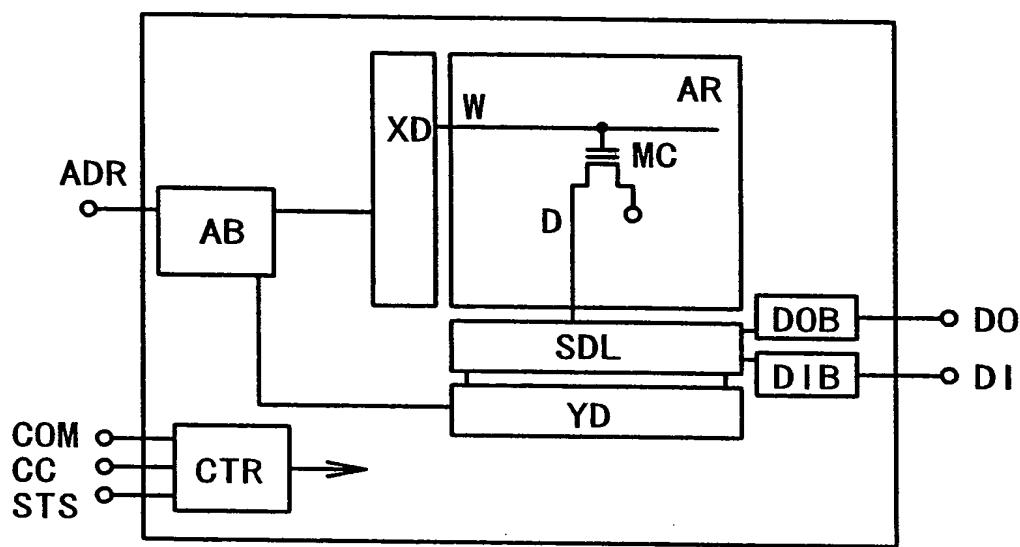


FIG. 11B

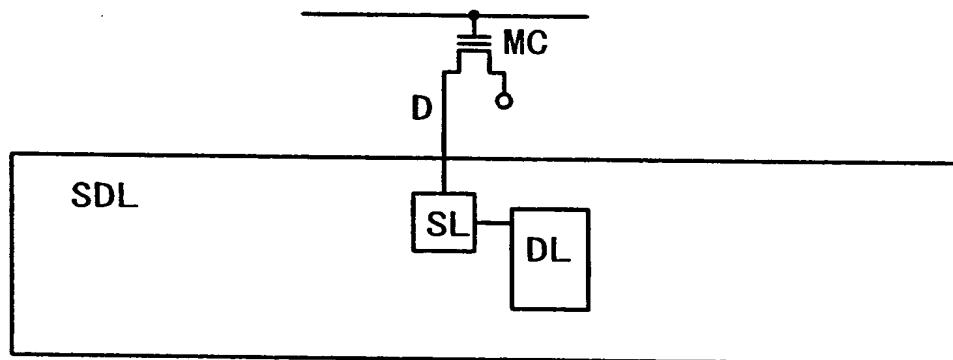


FIG. 12

